

IN THE CLAIMS

Cancel Claims 1 - 60 and amend Claims 61 and 65 so that the claims are as follows:

61. (Currently amended) A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurring in the body region and occupying a lateral inversion area along the primary surface, the inversion area reaching a maximum value when the inversion layer is fully present, the varactor having a maximum capacitance dependent on the maximum inversion area in combination ~~common~~ with the plate area, the plate electrode being at a plate-to-body voltage relative to the body electrode, the gate electrode being at a gate-to-body voltage relative to the body electrode, the inversion layer comprising multiple variably appearing inversion portions respectively characterized by corresponding different zero-point threshold voltages of like sign, each inversion portion appearing/disappearing when the gate-to-body voltage passes through the corresponding zero-point threshold voltage with the plate-to-body voltage at zero, each inversion portion meeting the plate region or/and being continuous with the another inversion portion whose zero-point threshold voltage is of lower magnitude than the zero-point threshold voltage of that inversion portion; and

adjusting the plate and maximum inversion areas to control the maximum and minimum capacitances of the varactor.

62. (Original) A method as in Claim 61 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to an accumulative combination of the plate and maximum inversion areas.

63. (Original) A method as in Claim 61 wherein the adjusting act involves adjusting the ratio of the maximum inversion area to the plate area in order to achieve at least a specified value of the ratio of the maximum capacitance to the minimum capacitance.

64. (Original) A method as in Claim 61 further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

65. (Currently amended) A method as in Claim 61 wherein the gate dielectric layer comprises multiple gate dielectric portions of different respective thicknesses, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions occurs.

66. (Original) A method as in Claim 61 wherein a surface depletion region of the body region extends along the gate dielectric layer below the gate electrode, the surface depletion region comprising multiple surface depletion portions of different respective average net dopant concentrations, each surface depletion portion situated below where a different corresponding one of the inversion portions occurs.

67. (Original) A method as in Claim 61 wherein the gate electrode comprises multiple gate electrode portions of semiconductor material, each gate electrode portion situated above at least where a different corresponding one of the inversion portions occurs, each gate electrode portion being of a different conductivity type or/and a different average net dopant concentration than each other gate electrode portion.

68. (Original) A method as in Claim 61 wherein:
the gate dielectric layer comprises a first gate dielectric portion and second gate dielectric portion thicker than the first gate dielectric portion, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions occurs;
and

the gate electrode comprises (a) a first gate electrode portion of semiconductor material of opposite conductivity type to the body region and (b) a second gate electrode portion of semiconductor material of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the second gate

electrode portion situated above at least where a further corresponding one of the inversion portions occurs.